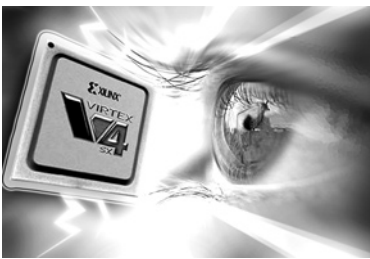


Hardware Algorithms for Iris Recognition Systems

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Iris recognition technology combines computer vision, pattern recognition, statistical inference, and optics. Its purpose is real-time, high confidence recognition of a person's identity by mathematical analysis of the random patterns that are visible within the iris of an eye. Because the iris is a protected internal organ whose random texture is stable throughout life, it can serve as a kind of living passport. As the randomness of iris patterns has a very high dimensionality, recognition decisions are made with high level of confidence.



Objective

The aim of our diploma work is to implement an image acquisition system and an iris recognition algorithm on an embedded FPGA system. The development platform is Xilinx's ML401 Development Board which features a Virtex-4 FPGA and provides a variety of interfaces like USB and RS232 and VGA. Instead of a hardware-implemented processor or microcontroller the board is powered by the Xilinx's Microblaze softcore processor residing in the FPGA and running at a clock frequency of 100 MHz.

Iris recognition algorithm

Image acquisition is the very first task when image recognition is performed. The image system is

designed around an ordinary webcam which provides a grey scale image with a resolution of 640 x 480 pixels. Once a usable image of the eye is available, the iris recognition algorithm performs the desired filtering and transformations to extract the iris pattern. The result of this multi-step image treatment is a dataset representing the human iris in a binary matrix. Comparing the scanned iris with an iris database allows identifying the person.

The filtering functions which are similar to the image transformation algorithms make exhaustive use of multiply and add operations. The algorithm was developed and optimized for workstations running under a 32 bit operation systems and a CPU running at a speed of more than 2 GHz. Our embedded development system is running at a clock speed of more than one decade under today's ordinary workstations CPUs. Parts of the iris detection algorithm are implemented in hardware to reach execution times comparable to normal computers.

Hardware Development

The Xilinx System Generator for digital signal processing (DSP) is a plug-in for the Simulink tool which enables designers to develop high-performance DSP systems for FPGAs. The tool provides libraries with configurable filters and mathematical functions which can be synthesized into hardware. Such hardware processing units can be connected via FIFOs to the 32-bit Microblaze RISC processor, allowing the processing of calculation-intensive algorithms with high speed and in parallel with the main RISC processor. Dividing algorithms in control-intensive software parts and processing-intensive hardware parts leads to a so called system-on-chip (SoC) architecture, which shows a superior processing power compared to software-only embedded systems. It has been shown in the literature that for dedicated applications SoC architectures may even outperform PC solutions in processing power.



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